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Invention: METHODS, APPARATUS, AND SYSTEMS FOR REDUCING INTERFERENCE ON NEARBY CONDUCTORS

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SPECIFICATION

METHODS, APPARATUS, AND SYSTEMS FOR REDUCING INTERFERENCE ON NEARBY CONDUCTORS

BACKGROUND

1. Field of the Invention

[0001] The present invention relates to information transmission. More specifically, the present invention relates to information transmission along conductive structures.

2. Background Information

[0002] Buses of parallel conductors are commonly used on circuit boards to carry data from one location to another. Problems associated with the use of such buses include delays incurred during propagation of the data signals and interference due to coupling of the conductors with one another.

[0003] Recently, it has become desirable to enable the use of buses of parallel conductors on small-scale structures such as within an integrated circuit ('chip'). While the propagation delay may be minimal in such applications, undesirable coupling effects become more problematic. For example, capacitive coupling may occur between the parallel conductors, contributing to an increased impedance at high frequencies that limits bandwidth and distorts signal features. Such problems may impose undesirable limits on the maximum clock speed, the minimum size and separation of the conductors, and/or the maximum length of the bus in a particular application.

[0004] Timing considerations are especially critical in high-speed integrated circuits currently under development. In these circuits the time between state

changes is minimal, and any fluctuation in the transition times may cause a delay that increases the error rate of the chip and decreases chip performance. In a chip clocked at 900 megahertz, for example, each cycle has a duration of only 1.1 nanosecond. If the time required to propagate a state transition across a transmission line is longer than a clock cycle, then the clock speed must be reduced.

[0005] As the conductors become more narrow and closer together, and as the time between state transitions decreases (e.g. as the clock speed increases), interference mechanisms that have negligible effects in other applications become limiting. In a 0.18-micron process, for example, with a pitch of 0.4 microns per wire, coupling effects may impede operation at any speed above a few hundred megahertz. For such reasons, chip designers commonly avoid long runs of parallel conductors in their designs.

[0006] One effect of coupling interference is an alteration of state transitions as they propagate over the conductors, resulting in a time skew of the signals being transmitted. When a new value is clocked onto a transmission line, an opposite current is induced in an adjacent (victim) transmission line. This induced current (or 'crosstalk') causes the skewing of a signal being transmitted on the victim line.

[0007] Timing within a circuit or assembly may be of critical importance: for example, when circuitry at the emitting and/or receiving sides of the transmission line is controlled by a clock (such as within an application-specific integrated circuit or 'ASIC'). In such cases, an altered rise time of a state transition may result in a loss of synchronization between different parts of the circuit and the failure of the chip to perform properly. For example, a skew in rise time may cause a state change to be detected at the receiving side at a different time than was intended because the threshold voltage was reached before or after the intended time.

[0008] One method of reducing the effect of crosstalk among signals on parallel conductors includes increasing the power of the signal before transmission. As a result of recent advancements in integrated circuit technologies, however, this method has become outdated. Reduction in integrated circuit feature dimensions, for example, require a consequent reduction in the power supply voltages in order to maintain acceptably low electric field intensities.

[0009] An alternative approach to reducing the effect of crosstalk is to shield each transmission line individually in order to reduce the degree of crosstalk between adjacent lines. However, this method is also not viable for chip design because such shielding reduces the amount of surface area available on the chip for transmission lines and other circuit elements. A method of adding additional lines with balanced current and voltage values to counteract the effects of crosstalk and increase the distance between adjacent signal lines suffers from the same problem, as the additional lines will also consume surface area on the chip.

[00010] Repeaters have been used along transmission lines to decrease the total transmission time to a level at which the skew of the signal is acceptable. In other words, because delay may be due to both the skewing of the state transition and the propagation time, a reduction in the propagation time may reduce the total delay to an acceptable level. Again, however, such a method requires additional surface area on the chip (for the repeaters). Although methods exist to minimize the amount of space required for the repeaters, space limitations are still of major concern to chip designers. Additionally, the signals outputted by the repeaters may still interfere with signals on nearby conductors.

[00011] Reductions of scale and increased speeds associated with new integrated circuit designs require new and innovative techniques to reduce interference during information transmission.

SUMMARY

[00012] In a method of data transmission according to one embodiment of the invention, data transitions on adjacent conductors are separated in time. One such method of data transmission includes receiving a plurality of sets of input signals, each input signal having a series of state transitions synchronized to a data clock signal that has a period T_CLK.

[00013] This method also includes transmitting a corresponding plurality of sets of output signals (in one example, the receiving and transmitting occur on the same semiconductor substrate). Each output signal corresponds to one of the input signals of the corresponding set and has a series of state transitions corresponding to the series of state transitions of that input signal. For example, each state transition of an output signal may correspond to a different state transition of the corresponding input signal.

[00014] Each output signal also passes along a corresponding one of a plurality of conductive paths. Adjacent conductive paths that each carry an output signal of one set are separated by at least one conductive path that carries a signal of another set. In one example, each conductive path includes a buffer.

[00015] Each conductive path may include a corresponding one of a plurality of transmission lines. For example, one of the transmission lines may carry a clock signal based on the data clock signal.

[00016] A time between a state transition on an input signal of one set and the corresponding state transition on the corresponding output signal is designated as T1. A time between a state transition on an input signal of another set and the corresponding state transition on the corresponding output signal is designated as T2. Time T1 exceeds time T2 by a delay period T_DLY, and the delay period is less than the clock period T_CLK. In one

example, the delay period is also at least twice as long as a rise time of the data clock signal.

[00017] Additional embodiments of the invention include data transmitters, data receivers, and systems including data transmitters and receivers.

BRIEF DESCRIPTION OF THE DRAWINGS

[00018] FIGURE 1 is a block diagram showing an application of a transmitter 10 according to an embodiment of the invention.

[00019] FIGURE 2 is an exemplary illustration of time relations between signals in the application of FIGURE 1.

[00020] FIGURE 3 is a block diagram of an application of an implementation 12 of a transmitter 10 according to an embodiment of the invention.

[00021] FIGURE 4 is an exemplary illustration of time relations between signals in the application of FIGURE 3.

[00022] FIGURE 5 is a block diagram of an application of an implementation 12 of a transmitter 10 according to an embodiment of the invention.

[00023] FIGURE 6 is a block diagram of an implementation 100 of a transmitter 10 according to an embodiment of the invention.

[00024] FIGURE 7 is a block diagram of an implementation 200 of a transmitter 10 according to an embodiment of the invention.

[00025] FIGURE 8 is a block diagram of an implementation 102 of a transmitter 10 according to an embodiment of the invention.

[00026] FIGURE 9 is a block diagram of an implementation 202 of a transmitter 10 according to an embodiment of the invention.

[00027] FIGURE 10 is a block diagram of an implementation 104a of a transmitter 10 according to an embodiment of the invention.

[00028] FIGURE 11 is a block diagram of an implementation 104b of a transmitter 10 according to an embodiment of the invention.

[00029] FIGURE 12 is a block diagram of an implementation 106 of a transmitter 10 according to an embodiment of the invention.

[00030] FIGURE 13 is a block diagram of an implementation 204 of a transmitter 10 according to an embodiment of the invention.

[00031] FIGURE 14 is a block diagram of an implementation 206 of a transmitter 10 according to an embodiment of the invention.

[00032] FIGURE 15 is a block diagram of an implementation 208 of a transmitter 10 according to an embodiment of the invention.

[00033] FIGURE 16 is a block diagram of an implementation 210 of a transmitter 10 according to an embodiment of the invention.

[00034] FIGURE 17 is a block diagram showing an application of a transmitter 10 and a receiver 112 according to an embodiment of the invention.

[00035] FIGURE 18 is a block diagram of an implementation 500 of a receiver 112 according to an embodiment of the invention.

[00036] FIGURE 19 is a block diagram of an implementation 502 of a receiver 112 according to an embodiment of the invention.

[00037] FIGURE 20 is a block diagram of an implementation 504 of a receiver 112 according to an embodiment of the invention.

[00038] FIGURE 21 is a block diagram of an implementation 506 of a receiver 112 according to an embodiment of the invention.

[00039] FIGURE 22 is a block diagram showing an application of a transmitter 14 according to an embodiment of the invention.

[00040] FIGURE 23A, 23B are illustrations showing transitions of signals transmitted on transmission lines that have opposite series of inverting and non-inverting buffers.

[00041] FIGURE 24 is a block diagram showing an application of a transmitter 14 according to an embodiment of the invention.

[00042] FIGURE 25 is a block diagram showing an application of a transmitter 14 according to an embodiment of the invention.

[00043] FIGURE 26 is a block diagram showing an application of an implementation 106a of a transmitter 10 according to an embodiment of the invention.

[00044] FIGURE 27 is a block diagram showing an application of an implementation 106b of a transmitter 10 according to an embodiment of the invention.

[00045] FIGURE 28 is a block diagram showing an application of two instances 16-1 and 16-2 of an implementation 16 of a transmitter 10 according to an embodiment of the invention.

[00046] FIGURE 29 is a block diagram showing an application of two instances 18-1 and 18-2 of an implementation 18 of a transmitter 10 according to an embodiment of the invention.

[00047] FIGURE 30 is a block diagram showing an application of two instances 300-1 and 300-2 of an implementation 300 of a transmitter 10 according to an embodiment of the invention.

[00048] FIGURE 31 is a block diagram showing an application of two implementations 300 and 302 of a transmitter 10 according to an embodiment of the invention.

[00049] FIGURE 32 is a block diagram showing an application of two instances 300-1 and 300-2 of an implementation 300 of a transmitter 10 according to an embodiment of the invention.

[00050] FIGURE 33 is a block diagram showing an application of two implementations 300 and 304 of a transmitter 10 according to an embodiment of the invention.

[00051] FIGURE 34 is a block diagram showing an application of two instances 16-1 and 16-2 of an implementation 16 of a transmitter 10 according to an embodiment of the invention.

[00052] FIGURE 35 is a block diagram showing an application of two instances 16-1 and 16-2 of an implementation 16 of a transmitter 10 according to an embodiment of the invention.

[00053] FIGURE 36 is a block diagram showing an application of two instances 306-1 and 306-2 of an implementation 306 of a transmitter 10 according to an embodiment of the invention.

DETAILED DESCRIPTION

[00054] Signal transmission on sets of conductors may be performed in several different contexts. Between circuit units or assemblies, for example, signals may be transmitted across distances of centimeters or meters on a ribbon cable or another cable having parallel conductors. In a printed circuit board, signals may be transmitted on parallel conductive traces across distances of millimeters or centimeters. In a semiconductor chip, signals may

be transmitted across distances of millimeters or microns on parallel conductive paths or structures that may be formed (e.g. deposited or etched) on a substrate.

[00055] As the characteristics of the signals (such as clock speed) change, effects that were negligible or undetectable in another application may become significant or even limiting. As signal frequencies increase, for example, capacitive effects may allow conduction between nearby conductors, resulting in crosstalk between signals.

[00056] Conductor dimensions may include the length, width, and thickness of each conductor; the feature pitch (characterizing the separation between conductors as measured on the substrate surface); and the vertical separation between conductors. As conductor dimensions and/or relations between those dimensions change, effects that were negligible or undetectable in another application may become significant or even limiting.

[00057] In wafer-scale-integration applications, for example, conductive paths less than one-half micron wide (and less than one-half micron apart) may extend in parallel buses that are dozens of centimeters long (i.e. for a length-to-width ratio of 10^6 or more). In one such application, a number of interconnected cells are fabricated on a single semiconductor substrate that may have a diameter of ten to thirty centimeters. One structure of this class (also called large-area integrated circuits or LAICs) holds an array of tens to thousands of cells that communicate over buses having dozens of conductive paths and lengths of ten to thirty centimeters. In one such example, a bus has forty parallel conductive paths and a length of up to twelve inches.

[00058] The signals transmitted on a set of conductors may have several different forms. For example, a portion of the set of conductors may form a parallel signal bus, with each conductor carrying a designated bit of a multi-bit information value (e.g. a byte or word). In another example, one or more of the conductors may carry data values serially. In a further example, one or

more of the conductors may carry other information such as parity or other error-control information, source and/or destination information, control values, a clock signal, etc.

[00059] In a method for reducing interaction between signals on nearby conductors according to one embodiment of the invention, data transitions on adjacent conductors are separated in time.

[00060] FIGURE 1 shows a block diagram of an application of an implementation 10 of a transmitter according to an embodiment of the invention. Transmitter 10 receives two sets of input signals S10a, S10b and transmits two sets of corresponding output signals S20a, S20b on a set of conductive paths 15. In an exemplary implementation, conductive paths 15 are parallel to one another.

[00061] A time T1 is defined as the period between a state transition on an input signal S10b and the corresponding state transition on the corresponding output signal S20b. A time T2 is defined as the period between a state transition on an input signal S10a and the corresponding state transition on the corresponding output signal S20a. In the application shown in FIGURE 1, time T2 exceeds time T1 by a delay period T_DLY.

[00062] FIGURE 2 shows a timing diagram for an exemplary application of transmitter 10 as shown in FIGURE 1. In this example, each signal S10 carries a series of binary values, with a transition from one value to the other being indicated by a state transition synchronous to a rising edge of a data clock signal. Relations between signals as shown in FIGURE 2 are presented by way of example only and are not intended to represent limitations on the practice of the invention or of the application shown in FIGURE 1.

[00063] FIGURE 3 shows a block diagram of an application of an implementation 12 of transmitter 10 according to an embodiment of the invention. In this application, transmitter 12 transmits each output signal S20

on a corresponding one of a set of parallel transmission lines 20. In one example, one or more of transmission lines 20 may include one or more buffers. These buffers (or repeaters) may be used to regenerate the signal and preserve signal bandwidth.

[00064] Transmitter 12 also receives a clock signal CLK0. Clock signal CLK0 may have a duty cycle of 50% with substantially equal rise and fall times, although such features are not required for practice of the invention. In one example, clock signal CLK0 has a period of 8 nanoseconds (ns) and a rise time of 1 ns.

[00065] FIGURE 4 shows a timing diagram for an exemplary application of transmitter 12 as shown in FIGURE 3. In this example, clock signal CLK0 has the same frequency as the data clock signal. In other applications, the data clock may be the same as clock signal CLK0. In further applications, one or more of the input signals S10 may be timed according to a different frequency or offset than another of the input signals S10. Relations between signals as shown in FIGURE 4 are presented by way of example only and are not intended to represent limitations on the practice of the invention or of the implementation shown in FIGURE 3.

[00066] In an exemplary implementation, delay period T_DLY is less than the period T_CLK of the data clock signal. In a further example, delay period T_DLY is at least two times the length of the rise time of the data clock signal.

[00067] FIGURE 5 shows a block diagram of an application of an implementation 12 of transmitter 10 according to an embodiment of the invention. In this application, clock signal CLK0 is transmitted on a transmission line 20c1 parallel to the transmission lines 20 that carry output signals S20. In another application, transmitter 12 transmits clock signal CLK0 onto transmission line 20c1.

[00068] FIGURE 6 shows a block diagram of an implementation 100 of transmitter 10. Transmitter 100 includes a set of first latches 110a that receive clock signal CLK0 and input signals S10a. In response to a specified state transition of clock signal CLK0 (e.g. a rising or falling edge), first latches 110a latch the data values on input signals S10a onto output signals S20a. First latches 110a may be implemented using flip-flops (e.g. as shown in FIGURE 6) and/or other sequential logic devices.

[00069] Transmitter 100 also includes a set of second latches 110b that receive clock signal CLK0 and input data signals S10b. Upon the specified state transition of clock signal CLK0, second latches 110b latch the data values on input signals S10b onto the inputs of delay elements 120. Second latches 110b may be implemented using flip-flops and/or other sequential logic devices. After a predetermined delay (which may be the same for all delay elements 120 or may differ among them), delay elements 120 impose the data values onto the respective output signals S20b.

[00070] Transmitter 100 produces output signals S20 for transmission across a set of conductive paths (e.g. as shown in FIGURES 1, 3, and 5), the output signals S20 being arranged such that adjacent conductive paths that carry outputs signals S20b are separated by at least one conductive path that carries an output signal S20a. In an exemplary application, no two output signals 20a are carried over adjacent conductive paths and no two output signals 20b are carried over adjacent conductive paths. Because transitions on the signals S20b are delayed with respect to those on the signals S20a, it may be understood that data transitions on adjacent conductors are separated in time.

[00071] It may be desirable to perform the time separation among the output signals S20 by inserting one or more delay elements into a clock path rather than (or in addition to) inserting delay elements into one or more signal paths. FIGURE 7 shows a block diagram of an alternative implementation 200 of a transmitter 100 according to an embodiment of the invention. Transmitter 200

includes a set of first latches 110a that receive a clock signal CLK0 and input data signals S10a. As above, in response to a specified state transition of clock signal CLK0 (e.g. a rising or falling edge), first latches 110a latch the data values on input signals S10a onto output signals S20a.

[00072] Transmitter 200 includes a delay element 220-1, which receives clock signal CLK0 and produces a clock signal D_CLK0 having a predetermined delay with respect to clock signal CLK0. Transmitter 200 also includes a set of second latches 110b that receive input data signals S10b and delayed clock signal D_CLK0. In response to a specified state transition of delayed clock signal D_CLK0, second latches 110b latch the data values on input signals S10b onto output signals S20b. In one implementation, delay element 220-1 introduces a predetermined delay that is variable (e.g. according to a control signal from a control unit).

[00073] In a transmitter according to implementation 100, it may be desirable for the delays introduced by delay elements 120 to have values at least twice the rise time of clock signal CLK0 and no greater than one-half of the period of clock signal CLK0. In a transmitter according to implementation 200, it may be desirable for delayed clock signal D_CLK to be delayed with respect to clock signal CLK0 by a value that is at least twice the rise time of clock signal CLK0 and no greater than one-half of the period of clock signal CLK0. Particular delay values may be selected for specific applications (e.g. based on simulations) to minimize interaction among transitions on the conductive paths.

[00074] As compared to transmitter 100, transmitter 200 may be constructed using fewer delay elements (in these particular examples, one delay element as compared to N/2 delay elements, where N is the total number of signal lines S10). Transmitter 200 may also exhibit a more uniform power consumption over time, as no more than half of the latches in transmitter 200 switch at any given time (for an application in which the number of output signals S20a

equals the number of output signals S20b). Additionally, for transmitter 200 as shown in FIGURE 7, the number of conductive paths is not a factor in the number of delays: regardless of the number of conductors, one delay is sufficient to achieve a separation in time of data transitions on adjacent conductors. This feature may support a longer life expectancy of transmitter 200 and/or of an integrated circuit that includes transmitter 200.

[00075] In some applications, it may be desirable to pass one or more of the output signals S20 through a buffer prior to transmission on the conductive paths (e.g. transmission lines). For example, a buffer 130 may be used to boost the signal to an acceptable level for the intended receiver or to reduce the impact of a capacitive load (e.g. as may be encountered in a long transmission line). FIGURES 8 and 9 show implementations 102 and 202 of transmitters 100 and 200, respectively, that include buffers 130. In an exemplary implementation, a buffer 130 is implemented as two consecutive inverters, with the second inverter outputting a stronger signal (e.g. having larger transistors) than the first inverter.

[00076] It may be desirable to increase the separation in space between data transitions that may interfere. For example, it may be desirable to increase the distance between conductive paths carrying similarly timed data transitions.

[00077] FIGURE 10 shows a block diagram of an implementation 104a of transmitter 10 according to an embodiment of the invention in which more than one other output signal S20 separates adjacent output signals S20 having the same clock dependence. In this example, output signals S20a are not delayed, output signals S20b are delayed (via delay elements 120b) by a first delay period, and output signals S20c are delayed (via delay elements 120c) by a second delay period that is longer than the first delay period. Further implementations may be configured to include output signals S20 having other delay periods, with the conductive paths being arranged to minimize signal interaction (e.g. in order of increasing delay periods as shown in FIGURE 10).

It may be desirable for the shortest delay period between adjacent conductors to have a value that is at least twice the rise time of clock signal CLK0 and for the longest delay period among the set of conductors to have a value that is no greater than one-half of the period of clock signal CLK0.

[00078] FIGURE 11 shows a block diagram of an alternative implementation 104b of a transmitter 104a as shown in FIGURE 10. In this example, the delay elements 120 all have the same delay period, such that output signals S20c are delayed by twice the delay period of output signals S20b.

[00079] In some cases, it may be desirable to have a uniform delay separation between the output signals on adjacent conductors. FIGURE 12 shows a block diagram of an implementation 106 of transmitter 100 according to an embodiment of the invention that has a time separation of one delay unit between output signals S20 on adjacent conductors (in this example, delay elements 120 all have the same delay period).

[00080] FIGURE 13 shows a block diagram of a transmitter 204 having multiple delayed clock signals D_CLK0, D2_CLK0 in which adjacent output signals S20 having the same clock dependence are separated by more than one other output signal S20. FIGURE 14 shows a block diagram of a transmitter 206 having multiple delayed clock signals whose output signals S20 have mutual time relations that are similar to those of the output signals S20 of transmitter 106 as shown in FIGURE 12.

[00081] One possible advantage of an implementation 204 of a transmitter as shown in FIGURE 13 is that each delay element may be loaded evenly (or nearly evenly), while in an implementation 206 of a transmitter as shown in FIGURE 14, an uneven delay element fanout may result. According to the particular application, buffers 130 as described above may optionally be used in implementations of transmitter 10 as shown in FIGURES 10–14.

[00082] It is possible but not necessary for the number of output signals S20 to be an integer multiple of the number of sets of latches in the transmitter. FIGURE 15 shows an example in which an implementation 208 of transmitter 10 having three sets of latches is arranged to drive an eight-bit bus.

[00083] Also, it is possible but not necessary for the delay elements to have equal delay periods, or for the delays between sets of latches to be equal. FIGURE 16 shows an example in which a unit delay separates the clock signals CLK0 and D_CLK0 driving latches 110a and 110b, respectively, while a two-unit delay separates the clock signals D_CLK0 and D3_CLK0 driving latches 110b and 110c, respectively. Other delay distributions may be implemented according to the particular application (e.g. as indicated by simulations). Also, buffers 130 as shown in FIGURES 15 and 16 may be optionally used according to the particular application.

[00084] FIGURE 17 illustrates an application according to an embodiment of the invention that includes a transmitter 12 and transmission lines 20 as described above. This application also includes a receiver 112 configured to receive output signals S20 and clock signal CLK0 and to produce received signals S60. Depending on factors such as a time relation between clock signal transitions at the transmitter and clock signal transitions at the receiver, the length of the delay between corresponding transitions on output signals S20a and S20b, and a desired relation between transitions on received signals S60, the implementation of receiver 112 may vary according to the particular application. In an exemplary application, state transitions on signals S60 are similarly timed with respect to each other.

[00085] As a consequence of a delay (whether inherent or deliberate) in transmitting a clock signal to receiver 112 (e.g. over one of the transmission lines), it may be possible to use a signal based on clock signal CLK0 to control the operation of latches 510 at the receiver. FIGURE 18 shows an implementation 500 of receiver 112 according to such an embodiment of the

invention. FIGURE 19 shows an alternate implementation 502 in which latches 512b are configured to latch upon the other transition of the clock signal.

[00086] FIGURE 20 shows an implementation 504 of receiver 112 according to another embodiment of the invention. In this implementation, a clock signal supplied to latches 510a is delayed by delay element 520-1 with respect to a clock signal CLK0 as supplied to latches 510b. In a case where output signals 20b are transmitted having a delay with respect to signals 20a (e.g. as described above), a net effect may be achieved in which receiver output signals S60a and S60b are essentially synchronous, have essentially the same time relation as they did before entering the transmitter, and/or have some other desired time relation.

[00087] It may be advantageous to delay the data signals at the receiver instead of delaying the clock signal, as clock delays may complicate downstream synchronous logic operations. FIGURE 21 shows an implementation 506 of receiver 112 according to an embodiment of the invention in which signals S20a are delayed by delay elements 520 before being inputted to latches 510a. As in the example of FIGURE 20, in a case where signals 20b are transmitted having a delay with respect to signals 20a, a net effect may be achieved in which receiver output signals S60a and S60b are essentially synchronous, have essentially the same time relation as they did before entering the transmitter, and/or have some other desired time relation.

[00088] A scheme of delaying a clock signal in the transmitter may be combined with a scheme of delaying alternating latch inputs in the receiver, and vice versa, and either such scheme may also be used in combination with a scheme of using rising and falling edges to control latches in the transmitter or receiver. Receivers as illustrated in FIGURES 18–21 may also be used with other implementations of transmitter 10 as described herein.

[00089] In a method for reducing interaction between signals on nearby conductors according to a further embodiment of the invention, signals on adjacent conductive paths pass through different alternating sequences of inversions and regenerations.

[00090] FIGURE 22 shows a block diagram of a system for data transmission according to an embodiment of the invention. Transmitter 10 produces a first set of output signals S30a and a second set of output signals S30b. A first set of conductive paths 17a receives the first set of output signals S30a, and a second set of conductive paths 17b receives the second set of output signals S30b. In an exemplary implementation, conductive paths 17 are parallel to one another.

[00091] Each of the conductive paths 17 includes a transmission line 22 that has a series of inverting buffers I and non-inverting buffers N. Inverting buffers I invert the state transitions of the signals they pass, and non-inverting buffers N regenerate the state transitions of the signals they pass. In the system shown in FIGURE 22, each of the transmission lines 22 has an alternating series of buffers, and the sequence of inversions and regenerations in the series of transmission lines 22a is different from (specifically, opposite to) the sequence in the series of transmission lines 22b.

[00092] When the same state transition occurs on two adjacent parallel conductors at substantially the same time (e.g. two rising edges), each transition tends to speed the propagation of the other along its respective transmission line. When opposite state transitions occur on two adjacent parallel conductors at substantially the same time (e.g. a rising and a falling edge), each transition tends to slow the propagation of the other along its respective transmission line.

[00093] In a typical application, the relations between transitions on adjacent transmission lines are not known *a priori*. For example, the data values being transmitted typically are not known beforehand. As the result, the slowing or

speeding of propagation of a particular transition due to nearby transitions becomes unpredictable, and an undesirable timing uncertainty may result.

[00094] In a system having an alternating and opposite arrangement of inversions and regenerations as shown in FIGURE 22, a transition passing from one end of a transmission line to the other will see the same (or nearly the same) number of similar state transitions and opposite state transitions on an adjacent transmission line. As described below, the system may be designed such that this condition is largely independent of the relation of the state transitions originally driven onto adjacent transmission lines 22, as is now described.

[00095] FIGURE 23A shows an example in which a similar state transition is transmitted over two nearby transmission lines 22a and 22b, and FIGURE 23B shows an example in which opposite state transitions are transmitted onto the two transmission lines. In the example of FIGURE 23A, transmitting a rising state transition over transmission lines 22a, 22b causes the following pairs of propagating transitions to appear on the segments of the two transmission lines (from left to right) after each of the four buffers:

[00096] falling/rising, falling/falling, rising/falling, rising/rising.

[00097] In the example of FIGURE 23B, transmitting a rising state transition over transmission line 22a and a falling state transition over transmission line 22b causes the following pairs of propagating transitions to appear on the segments of the two transmission lines (from left to right) after each of the four buffers:

[00098] falling/falling, falling/rising, rising/rising, rising/falling.

[00099] Although the pairs of propagating transitions appear in a different order in each case, one may see that in both cases, each of the four possible combinations occur once and only once. One may also see that the same is true for the other two possible input combinations (namely, a falling transition

over both lines, and falling and rising transitions on lines 22a and 22b, respectively). Therefore, each transition transmitted along one of these transmission lines will see the same combination of transitions on the other line, regardless of whether the transitions are rising or falling, or similar or different.

[000100] In an application where each transition along transmission lines 22 has the same magnitude, one may expect the effect of each transition along a transmission line to be substantially constant (i.e. with respect to transitions on nearby transmission lines). Therefore, it may be desirable to configure buffers I, N such that each buffer receives a transition of substantially equal magnitude. In implementing a system as shown in FIGURE 22, for example, it may be desirable for opposing buffers in adjacent transmission lines 22a, 22b (e.g. the pair of buffers I1a1 and N1b1) to be located at the same distance from transmitter 10.

[000101] It may also be desirable for each buffer to produce a transition of substantially equal magnitude. It may also be desirable to place the buffers of each transmission line such that each buffer receives transitions having one uniform magnitude and produces transitions having another uniform magnitude. For example, it may be desirable to have a uniform separation between the buffers of each transmission line 22.

[000102] As shown in FIGURE 24, the signals carried by the parallel conductors may be used to drive one or more other sets of parallel conductors. A possible advantage of one such system is that a set of parallel conductors may be tapped off of the transmission lines in a short space, permitting transitions on the tapped conductors to have substantially equal magnitudes as well. For example, in an application characterized by a line pitch of 0.4 microns, an eight-bit bus may be tapped off over a length of less than four microns.

[000103] FIGURE 25 shows a block diagram of a system for data transmission according to an embodiment of the invention. In this example, a pair of power rails 30a, 30b are situated parallel to and on opposite sides of the set of conductive paths 17a, 17b (here, including transmission lines 22). Power rails 30a, 30b may be coupled to provide an operating voltage to transmitter 10 and/or one or more of the buffers of transmission lines 22, or these components may be powered from another source. In an exemplary implementation, power rails 30a, 30b (carrying respectively Vcc and ground potentials) reduce interference by providing a well-defined return path for the signals transmitted across conductive paths 17a, 17b. The arrangement of power rails 30a, 30b as shown in FIGURE 25 may be used to similar effect in other embodiments described herein that include a plurality of conductive paths, such as those shown in FIGURES 1, 3, 5, 17, 22, and 29.

[000104] Data transitions having the same clock dependence may be further separated in space by combining a technique for separation in time between data transitions on adjacent conductors (e.g. as discussed above with reference to FIGURES 1–16) with a technique for passing signals on adjacent conductive paths through different alternating sequences of inversions and regenerations (e.g. as discussed above with reference to FIGURES 22–25).

[000105] To illustrate one such example, FIGURE 26 shows a combination of an application of a method according to an embodiment of the invention as shown in FIGURE 10 with an application of a method according to an embodiment of the invention as shown in FIGURE 22, such that similarly timed signals transmitted on adjacent conductive paths pass through different alternating sequences of inversions and regenerations. FIGURE 27 shows another such combination in which adjacent conductive paths carrying similarly timed signals include transmission lines having different alternating series of inverting and non-inverting buffers and are also separated by conductive paths carrying differently timed signals.

[000106] In a method for reducing interaction between signals on nearby conductors according to a further embodiment of the invention, data transitions having the same clock dependence are separated in space. In one such method, a first set of signals is transmitted in one direction on a first set of parallel conductors, and a second set of signals is transmitted in the opposite direction on a second set of parallel conductors that is interleaved with the first set.

[000107] FIGURE 28 shows a block diagram of an application of two instances 16-1, 16-2 of a transmitter according to an embodiment of the invention. In this application, transmitter 16 transmits output signals S40 on a set of conductive paths 32, and transmitter 16-2 transmits output signals S50 on a set of conductive paths 34. Conductive paths 32 and 34 are arranged such that adjacent conductors of one set are separated by at least one conductor of the other set. In an exemplary application, transmitter 16 is an implementation of transmitter 10 as described above.

[000108] FIGURE 29 shows a block diagram of an application of two instances 18-1, 18-2 of a transmitter according to an embodiment of the invention. In this application, each transmitter 18 transmits each output signal S40, S50 on a corresponding one of a set of conductive paths, each path including a parallel transmission line 26, such that lines carrying signals S40 are interleaved with lines carrying signals S50. Each transmitter 18 also receives the clock signal CLK0. In an exemplary application, transmitter 18 is an implementation of transmitter 10 as described above.

[000109] FIGURE 30 shows implementations 300-1 and 300-2 of a transmitter according to an embodiment of the invention that are applied to receive clock signal CLK0 and input signals S12, S14 (where n is arbitrarily large) and to transmit corresponding output signals S40, S50 in an interleaved fashion (e.g. as shown in FIGURE 28 and 29) over conductive paths (not shown). Each among the sets of input signals S12, S14 may be similar to input signals S10 as

described above. Each transmitter 300 includes a bank of latches 310, 312 that latch a value (e.g. state) received at an input onto an output upon a predetermined transition of clock signal CLK0.

[000110] In a system as shown in FIGURE 30, it may be desirable to avoid sending data transitions in both directions at once. For example, it may be desirable for a time separation between transitions on an output signal (e.g. S40) to exceed the time required for the signal to propagate from one end of the corresponding conductive path to the other.

[000111] A time separation between output signals S40 and S50 may be achieved at least in part as a consequence of an inherent delay in transmitting clock signal CLK0 (e.g. over one of a set of conductive paths 32 or parallel transmission lines 26) to transmitter 300-2. Alternatively, as shown in FIGURE 31, such separation between output signals S40 and S52 may be achieved by arranging latches 310 of one transmitter 300 to latch upon one of the transitions (e.g. the rising or falling edges) of clock signal CLK0 and arranging latches 314 of the other transmitter 302 to latch upon the other transition of clock signal CLK0.

[000112] FIGURE 32 shows a further application of transmitters 300-1 and 300-2 in which a difference in timing between output signals S40 and S52 is achieved at least in part by inserting a delay element 320 into the path of clock signal CLK0 to transmitter 300-2. Such a delay element, for example, may be incorporated into transmitter 300-2 and/or may receive clock signal CLK0 over one of a set of conductive paths carrying output signals S40, S52.

[000113] FIGURE 33 shows a block diagram of an application including implementations 300 and 304 of a transmitter according to an embodiment of the invention that are applied to receive input signals S12, S14 and transmit corresponding output signals S40, S52. In this case, the latch output signals of latches 312 are delayed by delay elements 330 before transmission over the conductive paths (not shown). Buffers as described above may also be

optionally used with transmitter implementations as shown in FIGURES 28–33.

[000114] Data transitions may be further separated by combining a technique for passing signals on adjacent conductive paths through different alternating sequences of inversions and regenerations (e.g. as discussed above with reference to FIGURES 22–25) with a technique for transmitting signals on interleaved sets of parallel conductors (e.g. as discussed above with reference to FIGURES 28–33). To illustrate one such example, FIGURE 34 shows a combination of a method according to an embodiment of the invention as shown in FIGURE 28 with a method according to an embodiment of the invention as shown in FIGURE 22. In this example, signals on adjacent transmission lines are transmitted in opposite directions, while adjacent transmission lines carrying signals in the same direction include different alternating series of inverting and non-inverting buffers. FIGURE 35 shows another such combination in which the transmission lines 22 are arranged in alternating pairs, each pair carrying signals in the same direction through different alternating series of inverting and non-inverting buffers.

[000115] Similarly timed data transitions may be further separated in space by combining a technique for separation in time between data transitions on adjacent conductors (e.g. as discussed above with reference to FIGURES 1–16) with a technique for transmitting signals on interleaved sets of parallel conductors (e.g. as discussed above with reference to FIGURES 28–33). To illustrate one such example, FIGURE 36 shows a combination of an application of a method according to an embodiment of the invention as shown in FIGURE 10 with an application of a method according to an embodiment of the invention as shown in FIGURE 29. This particular example also includes a delay element 320 as shown in FIGURE 32 implemented as an inverter 420.

[000116] In the example shown in FIGURE 36, the latches of transmitter 306-2 receive an inversion of clock signal CLK0. In another implementation,

inverter 420 may be included within the transmission line or within one of the transmitters. In an alternate implementation, latches of one transmitter (e.g. latches 110a1–110c3 of transmitter 306-1) are configured to latch upon one of the transitions of clock signal CLK0, while latches of the other transmitter (e.g. latches 110a4–110c6 of transmitter 306-2) are configured to latch upon the other transition of clock signal CLK0 (e.g. as shown in FIGURE 31).

[000117] Moreover, a technique for separation in time between data transitions on adjacent conductors (e.g. as discussed above with reference to FIGURES 1–16) may be combined with a technique for passing signals on adjacent conductive paths through different alternating sequences of inversions and regenerations (e.g. as discussed above with reference to FIGURES 22–25) and also with a technique for transmitting signals on interleaved sets of parallel conductors (e.g. as discussed above with reference to FIGURES 28–33).

[000118] Several different sequences of the individual conductive paths are possible for each such combination, e.g. as discussed with regard to the combinations described above. In one variation, for example, four adjacent conductive paths may carry differently timed signals in the same direction, while in another variation four adjacent conductive paths carry similarly timed signals in two different directions and through two different alternative sequences of inversions and regenerations. Simulations may be performed to determine the suitability of a particular combined scheme for a particular application.

[000119] The foregoing presentation of the described embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments are possible, and the generic principles presented herein may be applied to other embodiments as well. For example, the invention may be implemented in part or in whole as a hard-wired circuit or as a circuit configuration fabricated into an application-specific integrated circuit. Thus, the present invention is not intended to be

limited to the embodiments shown above but rather is to be accorded the widest scope consistent with the principles and novel features disclosed in any fashion herein.